

DOCKET NO.: 98-0957.01

**SUBSTITUTE SPECIFICATION  
(MARKED VERSION)**

**FOR**

**CAPACITOR STRUCTURE (as amended)**

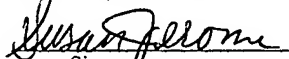
**INVENTORS:**

**Gurtej S. Sandhu  
Guy T. Blalock**

"Express Mail" MAILING LABEL NUMBER: ET658404685US

DATE OF DEPOSIT 7/3/03

I HEREBY CERTIFY THAT THIS PAPER IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED ABOVE AND IS ADDRESSED TO: MAIL STOP PATENT APPLICATION, COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450.

  
Signature

**Charles B. Brantley  
Registration No. 38,086  
Micron Technology, Inc.  
8000 S. Federal Way  
Boise, Idaho 83716-9632  
(208) 368-4557**

~~METHOD OF FORMING A CAPACITOR STRUCTURE~~ |

ABSTRACT OF THE DISCLOSURE

A capacitor structure and method of forming it are described. In particular, a high-K dielectric oxide is provided as the capacitor dielectric. The high-K dielectric is deposited in a series of thin layers and oxidized in a series of oxidation steps, as opposed to a depositing a single thick layer. Further, at least one of the oxidation steps is less aggressive than the oxidation environment or environments that would be used to deposit the single thick layer. This allows greater control over oxidizing the dielectric and other components beyond the dielectric. |

METHOD OF FORMING A CAPACITOR STRUCTURE

RELATED APPLICATION

[0001] This application is a divisional of U.S. App. Ser. No. 09/589,671, filed Jun. 7, 2000.

FIELD OF THE INVENTION

[0002] The present invention relates generally to a capacitor structure and its method of manufacture. More particularly, the present invention relates to a capacitor structure for high-density memory arrays.

BACKGROUND OF THE INVENTION

[0003] Without limiting the scope of the invention, its background is described in connection with prior methods of forming capacitor structures for dynamic random access memory (DRAM) using high-dielectric-constant materials (or high-K dielectrics). By high-dielectric-constant, it is meant a dielectric constant greater than 10 at room temperature, and preferably a dielectric constant greater than 20.

[0004] Advances in miniaturization of integrated circuits have led to smaller areas available for devices such as transistors and capacitors. For example, in semiconductor manufacture of a memory array for a DRAM, each memory cell comprises a capacitor and a transistor. In a conventional DRAM, pairs of memory cells are located within regions ("memory cell areas") defined by intersecting row lines ("word lines") and column lines ("bit lines" or "digit lines"). Accordingly, to increase memory cell density of the memory array, row lines and column lines are positioned with minimal spacing ("pitch"). Using minimal pitch in turn constrains memory cell area. In high-density memory array architecture, a memory array will have a bit line-to-bit line pitch equal to or less than 0.5 microns.

[0005] —In conflict with reducing memory cell area is maintaining a sufficient

amount of memory cell charge storage capacitance. Each DRAM memory comprises a capacitor for storing charge. A capacitor is two conductors separated by a dielectric, and its capacitance,  $C$ , is mathematically determinable as:

$$C = (\epsilon_r \epsilon_0 A) / d,$$

where  $\epsilon_0$  is a physical constant; dielectric constant,  $\epsilon_r$ , is a material dependant property; distance,  $d$ , is distance between conductors; and area,  $A$ , is common surface area of the two conductors.

[0006] To increase capacitance,  $C$ , per unit area, the DRAM industry is pursuing depositing materials with a high permittivity for use as capacitor dielectrics. Many perovskites, ferroelectrics, and other high-dielectric-constant materials have capacitance densities greater than standard silicon dioxide ( $\text{SiO}_2$ ) and silicon nitride ( $\text{Si}_3\text{N}_4$ ) capacitor dielectrics.

[0007] Many perovskites have the chemical formula  $\text{ABO}_3$ , where A is one or more monovalent, divalent, or trivalent elements and B is one or more pentavalent, tetravalent, trivalent, or divalent elements. Examples of high-dielectric-constant ferroelectric oxides include niobium pentoxide ( $\text{Nb}_2\text{O}_5$ ); tantalum pentoxide ( $\text{Ta}_2\text{O}_5$ ); and titanates including lead zirconate titanate ( $\text{PbTiZrO}_3$ , abbreviated PZT) and barium strontium titanate ( $\text{BaSrTiO}_3$ , abbreviated BST). Other high-dielectric-constant materials include but are not limited to non-oxide ferroelectrics, such as barium fluoride ( $\text{BaF}_2$ ) and magnesium fluoride ( $\text{MgF}_2$ ). Depending on the dielectric constant,  $\epsilon_r$ , of these materials, as well as the application, they may be used in parallel plate capacitor structures, such as stack capacitors or mini-stack capacitors, or vertical capacitor structures including container capacitors and trench capacitors.

[0008] High-dielectric-constant oxides are conventionally deposited in one step at elevated temperatures (greater than 500 degrees Celsius) in an oxygenated atmosphere (such as  $\text{O}_2$ ). Examples of processes for depositing high-dielectric-constant oxides are ion-beam sputtering, chemical vapor deposition, and pulsed laser deposition. It has been found that in such an environment, the capacitor electrode layer oxidizes, thereby

causing an unwanted reduction in capacitance. Moreover, such high-dielectric-constant oxides are often annealed or re-oxidized after deposition, which further exacerbates the oxidation problem.

[0009] In addition, other problems may occur if high-dielectric-constant oxide dielectrics are deposited directly on silicon (Si) capacitor electrodes. In addition to oxidation or other undesirable reactions between the electrode and dielectric, silicon may migrate into the high-dielectric-constant oxide, thereby reducing its permittivity and the capacitor's capacitance.

[0010] One option to at least partially prevent these problems is to provide a barrier layer, such as a layer of germanium (Ge) or silicon nitride ( $\text{Si}_3\text{N}_4$ ), between the silicon electrode and the high-dielectric-constant oxide. The oxidation conditions present after the deposition of this barrier layer may result in the oxidation of that layer, but this is actually preferable in certain circumstances. Regardless, it is desired in the art that this layer will prevent oxidation of the electrode. Unfortunately, the oxidation conditions in effect while forming the entirety of the high-K dielectric in one step often still cause oxidation of the silicon electrode despite the presence of the barrier layer. In addition, forming a barrier layer adds complexity to the manufacturing process and reduces the effective dielectric constant of the capacitor.

[0011] As an alternative to depositing dielectric on a silicon electrode, high-dielectric-constant oxides may be deposited on nonreactive metals or conductive metal oxides comprising the capacitor electrode. The term "nonreactive" when used in context with contact to a high-dielectric-constant oxide herein means a material that provides a stable conductive interface during and after processing. Examples of nonreactive metals include noble metals such as lead (Pd) or platinum (Pt). Exemplary conductive metal oxides include ruthenium oxide ( $\text{RuO}_2$ ). Single and multiple metal layers may be used to form the capacitor electrode. However, while this solves some of the problems associated with silicon electrodes, the problem of oxidizing the electrode during or after the formation of the high-K dielectric still exists.

[0012] As a result, it would be desirable to form a high-dielectric-constant oxide such that the likelihood of decreasing capacitance is reduced.

#### SUMMARY OF THE INVENTION

[0013] —Accordingly, the present invention provides a dielectric for a capacitor structure or other device, and method of formation thereof. Rather than provide a single layer of dielectric under a particular set of oxidation parameters, one exemplary embodiment of the current invention instead provides a plurality of thinner dielectric layers, wherein providing at least the layer nearest the capacitor electrode is accomplished under less aggressive oxidizing parameters. Such exemplary embodiments allow for greater control over the oxidation that may occur beyond the dielectric.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Features and advantages of the present invention will become more apparent from the following description of the preferred embodiments described below in detail with reference to the accompanying drawings where:

[0015] —FIGs. 1A and 1B are cross-sectional views of in-process DRAM substrate assemblies of the prior art.

[0016] FIGs. 2A and 2B are cross-sectional views of exemplary embodiments in accordance with the present invention.

[0017] FIGs. 3A and 3B are cross-sectional views of exemplary embodiments in accordance with the present invention having undergone additional processing.

[0018] —Reference numbers refer to the same or equivalent parts of embodiments of

the present invention throughout the several figures of the drawing.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0019] —In the following detailed Description of the Preferred Embodiments section, reference is made to the accompanying drawings which form a part of this disclosure, and which, by way of illustration, are provided for facilitating understanding of the exemplary embodiments. It is to be understood that embodiments other than the exemplary embodiments disclosed herein may be practiced without departing from the scope of the present invention. The following exemplary embodiments, directed to manufacture of dynamic random access memories (DRAMs), are provided to facilitate understanding of the present invention. Accordingly, some conventional details with respect to manufacture of DRAMs have been omitted to more clearly describe the exemplary embodiments herein.

[0020] —Referring to FIG. 1A, there is shown a cross-sectional view of an in-process DRAM substrate assembly 10 of the prior art. By substrate assembly, it is meant a substrate comprising one or more layers formed thereon or therein. Further, in the current application, the term “substrate” or “semiconductor substrate” will be understood to mean any construction comprising semiconductor material, including but not limited to bulk semiconductive materials such as a semiconductor wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). Further, the term “substrate” also refers to any supporting structure including, but not limited to, the semiconductive substrates described above. Substrate assembly 10 comprises a slice of a single crystalline semiconductor 11. In semiconductor 11, a well 12 is formed. In well 12 are formed conductive implant regions 14. Shallow trench isolation regions 13 are formed in semiconductor 11 by removing a portion thereof and filling the remaining hole with one or more dielectric materials. Transistor gate stacks 16 are formed on semiconductor 11, and are separated from conductive studs 15 by spacers 17. Dielectric layers 18 and 19 are deposited and etched to provide holes for deposition of conductive layer 20.

[0021] Conductive layer 20 is then polished to form a planar surface. As chemical-mechanical-polishing (CMP) is conventionally used for such polishing, photosensitive polymer 21 is deposited to protect substrate assembly 10 from potential contaminants associated with CMP. Conductive layer 20 provides bottom electrodes for container capacitor structures.

[0022] —Dashed-lines 5 indicate a proximate location for a contact via for connection to a conductive stud 15 therebelow. Separation 7 between dashed-lines 5 and outer surface 9 of conductive layer 20 bottom electrodes is about or less than 0.1 microns for a high-density DRAM array.

[0023] —Notably, though an exemplary embodiment of the present invention is described herein in terms of a container capacitor structure for a high-density DRAM array, it should be understood that the present invention may be employed to form container, stack, mini-stack, trench, or other capacitor structures in DRAM devices or in devices other than DRAM. The present invention may be implemented in a variety of other integrated circuit devices including but not limited to memory devices, logic devices having embedded memory, application specific integrated circuits, microprocessors, microcontrollers, digital signal processors, and the like incorporating a memory array which employs one or more capacitors. Moreover, a memory or a memory module having a capacitor formed in accordance with the present invention may be employed in various types of information handling systems. Such systems include network cards, telephones, scanners, facsimile machines, routers, televisions, video cassette recorders, copy machines, displays, printers, calculators, and personal computers, and the like systems incorporating memory.

[0024] Again, referring to FIG. 1A, conductive layer 20 provides a first electrode for a capacitor structure; in the exemplary embodiment illustratively shown, it is a container capacitor structure; however, conductive layer 20 may be thought of as a bottom electrode for any form of capacitor. Conductive layer 20 may be formed of one or



more layers of one or more materials. An optional barrier layer 4 may be formed between conductive layer 20 and conductive stud 15 to limit unwanted effects due to diffusion. Examples of oxygen diffusion limiting barrier materials that are conductors include metal nitrides, conductively formed semiconductors (*e.g.*, germanium doped with a material designated as an electron acceptor or an electron donor), and conductively formed semiconductor nitrides (*e.g.*, silicon nitride doped with a material designated as an electron acceptor or an electron donor). This barrier layer 4, however, does not limit or prevent unwanted effects of interaction between conductive layer 20 and a subsequently deposited high-dielectric-constant capacitor dielectric. As a result, another barrier layer 3, such as the one described in the background section and pictured in FIG 1B, may be provided between these layers.

[0025] With respect to these examples, oxidation of the conductive layer 20 will occur during or after a one-step formation of the full amount of high-K dielectric that will be used in the completed capacitor. By way of example and not limitation, if conductive layer 20 comprises silicon and a high-dielectric-constant oxide is deposited on it, then silicon dioxide may be formed. In addition, oxygen may reach other layers under the conductive layer 20 and create undesirable effects in other materials. Further, other undesirable reactions or material migrations may also occur.

[0026] —To mitigate unwanted interaction, the present invention offers exemplary embodiments that allow for formation of a high-K dielectric under conditions that minimize if not completely prevent oxidation beyond the dielectric. Rather than form the entire amount of dielectric at once under a given set of parameters, exemplary embodiments teach forming the dielectric in a plurality of steps, wherein each step provides only a portion of the total dielectric to be used in the completed device. Moreover, at least a first oxidation step involved with providing the dielectric is carried out under parameters that result in less aggressive oxidation in comparison to the prior art parameters.

[0027] Referring to FIG. 2A, there is shown a cross-sectional view of an in-process

DRAM substrate assembly 10A in accordance with the present invention. Conductive layer 20 may comprise an acceptor or donor doped semiconductor, platinum, palladium, rhodium, gold, iridium, silver, titanium nitride, tin nitride, ruthenium nitride, zirconium nitride, ruthenium dioxide, tin oxide, titanium monoxide, and combinations thereof. FIG. 2B illustrates an alternative exemplary portion of a substrate assembly 10B, wherein conductive layer 20 comprises hemispherical-grain-silicon having phosphorous added thereto for conductivity. Also added to the substrate assembly 10B is a silicon nitride barrier layer 3.

[0028] —In either embodiment, a first layer 22 of capacitor dielectric 24 is subsequently formed. First layer 22 may be formed at least in part by chemical-vapor-deposition (CVD), physical-vapor-deposition (PVD), jet-vapor deposition (JVD), liquid deposition (*e.g.*, spin-on, liquid injection, and the like), atomic layer deposition/epitaxy (ALD/ALE), or other means for controlled deposition of a material. Further, it should be noted that at least one oxidation step is used in providing many kinds of capacitor dielectric both in prior art and in exemplary embodiments of the current invention. For instance, oxidation may play an integral part of the initial deposition process so that an oxide is formed as a direct result of that process. Directly depositing a tantalum oxide is one example. Alternatively, a non-oxide may be initially deposited, followed by an oxidation step. Depositing tantalum and then oxidizing that layer into tantalum oxide serves as an example of this alternative process. Regardless of the method used to provide the oxide, such an oxide is often later subjected to an anneal in an oxidizing ambient in order to fill oxygen vacancies and burn away impurities in the oxide. Any of these oxidation steps can take place by way of one or a combination of oxidizing methods.

[0029] —Many of these oxidizing methods involve subjecting the substrate assembly 10A/10B to a thermal process in an oxygen containing atmosphere. Such an atmosphere may contain a gas including O<sub>2</sub>, O<sub>3</sub>, N<sub>2</sub>O, NO, H<sub>2</sub>O, or combinations thereof. The thermal energy can be provided in a furnace, wherein resistance to the conduction of electricity through the furnace coils generates the heat for the substrate

assembly 10A/10B. As another option, the substrate assembly 10A/10B could be placed in a rapid thermal process device such as the Centura HT tool, sold by Applied Materials, set to RTO (rapid thermal oxidation) mode. In such a device, a lamp shines light on the substrate assembly 10A/ 10B, which heats in reaction to absorbing the light. Alternatively, a reactor could be used to generate an oxygen-containing plasma, remote or local, for the substrate assembly 10A/ 10B. As yet another option, an anodic oxidation process using an electrolytic solution could be used to provide the oxidizing environment.

[0030] Returning to the tantalum oxide example, prior art indicates that it is known to deposit, in one step, 50 to 70 Angstroms of tantalum oxide. Exemplary parameters for doing so involve a CVD process wherein a tantalum precursor such as tantalum chloride ( $\text{TaCl}_5$ ) is carried by a gas such as argon into a furnace at a rate of 10 sccm to 2000 sccm. Further, an oxygen-containing gas such as  $\text{N}_2\text{O}$  is introduced to the furnace at a rate of 0.1 SLM to 5 SLM. The pressure inside the furnace is at 0.1 Torr to 10 Torr, and the temperature inside the furnace ranges from 800°C to 850°C. Under parameters such as these, the full amount of tantalum oxide will form after about 30 minutes. In contrast, an exemplary embodiment of the current invention involves providing a first layer 22 of tantalum oxide whose thickness is within the range of 10 to 40 Angstroms (preferably 20 Angstroms), wherein deposition can occur in the same furnace and with the same atmosphere but at a lower temperature -- ranging from 400°C to less than 800°C (preferably around 450°C) -- and a process time of about 1 minute. Thus, assuming that it is desired to ultimately have a dielectric thickness of 50-70 Angstroms, this exemplary embodiment teaches initially providing about 14% to 80% of that total.

[0031] —As another example, BST can be deposited as the first layer 22. Prior art teaches providing a full 200 Angstroms at 650°C. Embodiments of the current invention allow for initially providing a first layer 22 comprising BST, wherein the thickness ranges from 20-80 Angstroms and the temperature is less than 650°C, preferably between 400°C and less than 650°C. Assuming that it is desired to

ultimately have a dielectric thickness of 200 Angstroms, this exemplary embodiment teaches initially providing about 10% to 40% of that total.

[0032] —As a third example, it is assumed that a Metal-Insulator-Metal (MIM) capacitor configuration is desired, wherein tantalum pentoxide Ta<sub>2</sub>O<sub>5</sub> serves as the insulator. Prior art involves deposition parameters such as an ozone ambient and a temperature of 500°C, wherein the parameters result in the full amount of high-K dielectric being deposited. Exemplary embodiments of the current invention allow for less than the full amount of high-K dielectric to be initially deposited under less aggressive oxidation conditions in terms of time, temperature, pressure, oxygen source, other ambient gasses, or any other parameter.

[0033] —These examples demonstrate that the oxidation environment used during or after the deposition of the full amount of high-K oxide to be used in the capacitor results from a cooperation of several parameters, including the ones specified above as well as others such as the presence of excitation sources (like plasma or UV radiation) and their associated values. The current invention includes within its scope exemplary embodiments wherein less than the full amount of high-K oxide is initially provided, and oxidation associated with that initial amount is less than the oxidation that occurs in relation to depositing the full amount. The oxidation may occur during the deposition of an oxide dielectric, after the deposition of a non-oxide layer, or after the oxide has been provided. The oxidation may occur by way of any known method of oxidation, such as RTO, furnace oxidation, or other methods described above. The lesser oxidation is achieved by altering the oxidation parameters, such as in the ways described above as well as others.

[0034] —After depositing and oxidizing first layer 22, second layer 23 of capacitor dielectric 24 is formed, as illustratively shown in the cross-sectional views of FIGs. 3A and 3B. Second layer 23 can be formed in a manner similar to that of the first layer 22. However, that is not a requirement under the current invention. Second layer 23 may be deposited with different oxidation parameters in effect during or after

deposition. Further, it is not necessary that the oxidation parameters for the second layer 23 be less aggressive than those for the first layer 22. Returning to the MIM example, the second layer 23 of Ta<sub>2</sub>O<sub>5</sub> can be deposited at a temperature ranging from 400°C to 700°C. Thus, the oxidation parameters can exceed even those used in the prior art to oxidize the full amount of high-K dielectric deposited in one step. In addition, second layer 23 may be provided to define a thickness differing from the thickness of the first layer 22. Moreover, the type of high-K dielectric may be different from the high-K dielectric forming the first layer 22 in terms of the types of high-K dielectric components or their proportion.

[0035] High-dielectric-constant materials that may be used include perovskites, ferroelectrics, high-dielectric-constant oxides, acceptor doped perovskites, acceptor doped ferroelectrics, acceptor doped high-dielectric-constant oxides, donor doped perovskites, donor doped ferroelectrics, donor doped high-dielectric-constant oxides, and combinations thereof. The high-dielectric-constant material may be doped with a material selected from: Na, Al, Mn, Ca, La, Nb, F, K, Cr, Mn, Co, Ni, Cu, Zn, Li, Mg, Cl, V, Mo, Ce, Pr, Nd, Sn, Eu, Gd, Tb, Dy, Ho, Er, Ta, W, and combinations thereof.

[0036] —By repetitively forming sub-layers of capacitor dielectric 24, a desired thickness may be achieved while allowing greater control of the oxidation process than one would have by forming one layer of capacitor dielectric having that thickness. In embodiments such as the one depicted in FIG. 3A, oxidation may be generally restricted to the capacitor dielectric 24, thereby leaving the conductive layer 20 substantially free of oxide. A similar result may be achieved in the exemplary embodiment depicted in FIG 3B, but it would be preferred to allow oxidation to extend to the barrier layer 3 while still leaving the conductive layer 20 substantially free of oxide. The above described methods allow such a result.

[0037] —After forming a plurality of sub-layers of capacitor dielectric 24, conductive layer 25 may be deposited to provide a top electrode portion for capacitor 8. Conductive layer 25 may comprise acceptor doped silicon, donor doped silicon,

copper, aluminum, platinum, palladium, rhodium, gold, iridium, silver, titanium nitride, tin nitride, ruthenium nitride, zirconium nitride, ruthenium dioxide, tin oxide, titanium monoxide, and combinations thereof.

[0038] —It should be understood that substrate assembly 10A of FIGs. 2A, 2B, 3A and 3B may be formed in a single chamber 100 or in a cluster of chambers 100 without breaking vacuum. It should be understood that though only two sub-layers 22 and 23 are described herein, the present invention may be employed to provide two or more sub-layers for forming capacitor dielectric layer 24.

—The present invention has been particularly shown and described with respect to certain preferred embodiments. However, it will be readily appreciated to those of ordinary skill in the art that a wide variety of alternate embodiments, adaptations or variations of the preferred embodiments, and/or equivalent embodiments may be made without departing from the intended scope of the present invention as set forth in the appended claims. For example, the thickness of the initially deposited dielectric sub-layer can be as little as the thickness of one atom comprising that layer (in which case the sub-layer would be considered to be a “monolayer”) depending upon the tendency of subsequent processing steps to encourage oxygen diffusion. Further, it should be understood that exemplary embodiments of the current invention have applications in metal-insulator-silicon (MIS) structures as well as MIM structures discussed above and other structures known in the art. For instance, at least one exemplary embodiment of the current invention allows for an MIS device comprising a top metal electrode, a top Ta<sub>2</sub>O<sub>5</sub> layer under the top metal electrode, a bottom Ta<sub>2</sub>O<sub>5</sub> layer under the top Ta<sub>2</sub>O<sub>5</sub> layer, a silicon nitride layer under the bottom Ta<sub>2</sub>O<sub>5</sub> layer, and a bottom silicon electrode under the silicon nitride layer. In addition, the current invention is not limited to providing a capacitor dielectric. Rather, the invention has applications in any circumstance wherein controlling the oxidation of a dielectric or other insulator layer is beneficial. Accordingly, the present invention is not limited except as by the appended claims.